FREQUENCY AND PHASE CORRECTION IN A PHASE-LOCKED LOOP (PLL)

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to electronic circuits and more particularly to frequency and phase correction in a PLL.

BACKGROUND

Oscillators are often used in circuit design to generate signals having specific frequencies. Known oscillators include voltage-controlled oscillators with inductance-capacitance (LC) components. Using LC components, however, may result in a large circuit with high power consumption. Other known oscillators include current-controlled oscillators. These known oscillators, however, may be overly sensitive to external conditions.

SUMMARY OF THE INVENTION

According to the present invention, disadvantages and problems associated with PLLs may be reduced or eliminated.

In one embodiment, a system for frequency and phase correction in a phase-locked loop (PLL) includes a phase frequency detector, first and second charge pumps respectively generating a first current and a voltage, a voltage-to-current (V2I) converter, a current summer, and a current-controlled oscillator (CCO). The phase frequency detector detects a frequency difference and a phase difference between a clock signal and a comparison signal, communicates the frequency difference to a first charge pump generating a first current, and communicates the phase difference to a second charge pump generating a voltage. The comparison signal is derived from an output signal of the PLL. The first charge pump modifies the first current according to the frequency difference and communicates the first current to the current summer. The second charge pump modifies the voltage according to the phase difference and communicates the voltage to the V2I converter. The V2I converter generates a second current corresponding to the voltage and communicates the second current to the current summer. The current summer combines the first and second currents with each other to generate a control current for the CCO and communicates the control current to the CCO. The CCO generates one or more oscillating signals according to the first and second currents. A frequency of an oscillating signal from the CCO changes in response to the modification of the first current, and a phase of the oscillating signal changes in response to the modification of the second current.

Particular embodiments of the present invention may provide one or more technical advantages. As an example, particular embodiments may enable a PLL to facilitate voltage scaling. As a result, the PLL may function properly at relatively low power-supply voltages, such as 0.5 volts. Particular embodiments are scalable with respect to a power supply voltage, such as V_{DD}. In particular embodiments, components of the PLL are implemented such that the PLL may be scalable with

complementary metal-oxide semiconductor (CMOS) technology. Particular embodiments provide a feed-forward architecture. In particular embodiments, control current facilitates implementation of a feed-forward architecture. In particular embodiments, bias generation facilitates implementation of a feed-forward architecture.

Particular embodiments may, compared with LC tank oscillators, reduce area requirements associated with a PLL. Particular embodiments are readily configurable for clock dithering, which may reduce power output of the PLL and thereby reduce interference from the PLL that might affect circuit elements (such as antennas) near the PLL. In particular embodiments, oscillator gain is substantially independent of process and temperature. Particular embodiments are configurable for high performance and low power applications. Certain embodiments may provide all, some, or none of these technical advantages. Certain embodiments may provide one or more other technical advantages, one or more of which may be readily apparent to those skilled in the art from the figures, descriptions, and claims herein.

BRIEF DESCRIPTION OF THE DRAWINGS

To provide a more complete understanding of the present invention and the features and advantages thereof, reference is made to the following description, taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates an example PLL with frequency and phase correction;

FIGURE 2 illustrates, in greater detail, an example PLL with frequency and phase correction;

FIGURE 3 illustrates an example current-controlled oscillator (CCO) element;

FIGURE 4 illustrates an example method for frequency correction in a PLL; and

FIGURE 5 illustrates an example method for phase correction in a PLL.

DESCRIPTION OF EXAMPLE EMBODIMENTS

FIGURE 1 illustrates an example PLL 10 with frequency and phase correction. In one embodiment, PLL 10 includes a phase frequency detector 12, a proportional integral (PI) controller 14, a current summer 16, a CCO 18, one or more converters 20, and a divider 22. The components of PLL 10 may be coupled to each other using one or more wires, leads, or other suitable links. As an example, the components of PLL 10 may be coupled to a circuit board with embedded wires for coupling the components of PLL 10 to each other. Applications of PLL 10 include, for example, low-power, high-performance digital signal processor (DSP) cores, low-power wireless application-specific integrated circuits (ASICs), low-power serializer-deserializer (SERDES) interfaces, and other suitable applications.

PLL 10 may receive a clock signal 24 having a first frequency and, using clock signal 24, generate one or more PLL output signals 26 that each have a second frequency that is a multiple of the first frequency. As an example, PLL 10 may receive a clock signal 24 of approximately 60-70 MHz and, using clock signal 24, generate one or more output signals 26 of approximately 2.4 GHz. PLL 10 may receive clock signal 24 at phase frequency detector 12. Phase frequency detector 12 may compare clock signal 24 with a comparison signal 28 from divider 22 and determine, based on the comparison, a phase difference and a frequency difference between clock signal 24 and comparison signal 28, according to a suitable technique. Phase frequency detector 12 may generate a control signal 30 according to the phase and frequency differences and communicate control signal 30 to PI controller 14. As described below, PI controller 14 may generate two currents 32a and 32b based on control signal 30 and communicate currents 32 to current summer 16. Current 32a may correspond to a frequency difference between clock signal 24 and comparison signal 28, and current 32b may correspond to a phase difference between clock signal 24 and comparison signal 28.

Current summer 16 may combine currents 32a and 32b with each other and communicate a resulting control current 34 to CCO 18. In particular embodiments,

CCO 18 may include one or more CCO elements (which may include delay cells) that each generate two sinusoidal oscillating signals 36 that have phases that are approximately 180° apart from each other. Each CCO element of CCO 18 may be coupled to a converter 20 that converts sinusoidal waves into square waves, according to a suitable technique. Converter 20 may receive oscillating signals 36 from CCO element 44 and, using oscillating signals 36, generate two square waves that have duty cycles of approximately fifty percent and phases that are approximately 180° apart from each other. Output signals 26 of PLL 10 may include these (and possibly other) square waves. PLL 10 may generate one or more output signals 26. In particular embodiments, all output signals 26 have frequencies that are approximately equal to each other. Phases of output signals 26 may be different from each other. In particular embodiments, phases of output signals 26 may be evenly spaced around 360°. As an example, if PLL 10 generates twelve output signals 26, output signals 26 may have phases at 0°, 30°, 60°, 90°, 120°, 150°, 180°, 210°, 240°, 270°, 300°, and 330°.

A feedback signal 38 (which may include one or more output signals 26 of PLL 10) may be communicated from one or more converters 20 to divider 22. Divider 22 may receive feedback signal 38 and divide the frequency of feedback signal 38 according to a suitable technique to generate comparison signal 28 for phase frequency detector 12. As an example and not by way of limitation, if output signals 26 are intended to have frequencies that are each approximately one hundred times greater than the frequency of clock signal 24, divider 22 may divide the frequency of feedback signal 38 by one hundred to generate comparison signal 28. If a frequency difference exists between clock signal 24 and comparison signal 28, phase frequency detector 12 may communicate the frequency difference to PI controller 14 to cause PI controller 14 to modify current 32a (and therefore control current 34) to reduce the frequency difference, as described below. Similarly, if a phase difference exists between clock signal 24 and comparison signal 28, phase frequency detector 12 may communicate the phase difference to PI controller 14 to cause PI controller 14 to

modify current 32b (and therefore control current 34) to reduce the phase difference, as described below.

FIGURE 2 illustrates, in greater detail, example PLL 10. In particular embodiments, the lower limit of V_{DD} may be the threshold voltage of N-channel metal oxide semiconductor (NMOS) devices in PLL 10. In these NMOS devices, $V_{DD} > V_T + V_{DS}$ where V_T is threshold voltage and V_{DS} is saturation voltage. In particular embodiments, an upper limit of V_{DD} may be determined according to an upper power-supply voltage limit (such as 1.2V) of transistors in PLL 10. PI controller 14 includes two charge pumps 40a and 40b and a voltage-to-current (V2I) converter 42. Charge pump 40a generates a current (I_{PROP}) that is proportional to a frequency difference between clock signal 24 and comparison signal 28. Current 32a may include I_{PROP}. Charge pump 40b generates a voltage (V_{INT}) that is proportional to a phase difference between clock signal 24 and comparison signal 28. V2I converter 42 converts V_{INT} into a current (I_{INT}) that is proportional to this phase difference. Current 32b may include I_{INT}. I_{PROP} and I_{INT} are used to correct the frequency and phase differences, respectively. At current summer 16, I_{PROP} is superimposed onto I_{INT}. The combined current ($I_{PROP} + I_{INT}$) is then used to drive CCO 18. If the frequency of an output signal 26 becomes greater or less than an intended multiple of the frequency of clock signal 24, I_{PROP} may change to reduce this frequency difference. Similarly, if the phase of an output signal 26 shifts away from a phase of clock signal 24, I_{INT} may change to reduce this phase difference.

V2I converter 42 may integrate current I_1 to generate current I_{INT} according to the following two equations:

$$(1) \qquad V_{INT} \approx \frac{1}{C_1} \int I_1 dt$$

$$(2) \qquad I_{INT} = \frac{V_{INT}}{R}$$

Resistance R in V2I converter 42 may be trimmable, according to particular needs. R and Capacitances $C_1$and C_2 collectively provide a transform, as shown in the following equation:

$$(3) \qquad I_{BIAS} = f\left(\frac{\int I_1 \cdot dt}{RC_1}, I_{PROP}\right) = \frac{\int I_1 \cdot dt}{RC_1} \cdot \frac{g_m + 2s \cdot C_2}{g_m + s \cdot C_2} + I_{PROP} \cdot \frac{g_m}{g_m + s \cdot C_2}$$

In Equation 3, g_m represents transconductance of metal oxide semiconductor field effect transistor (MOSFET) Mg_m coupled to control current 34 and s represents a frequency of operation. If C_2 is greater than zero, PLL 10 is a third-order PLL 10. However, if C_2 becomes approximately zero, PLL 10 will become a second-order PLL 10. C_1, C_2, C_{PSRR}, and R may collectively dampen ringing that may occur in phase and frequency shifts in the output signal of the PLL. C_2 provides a third-order term to Equation (3), and, when C_2 is greater than zero, the output signal of the PLL may flatten out sooner after a phase shift, frequency shift, or both.

Loop gain G(s) of PLL 10 may be calculated as follows:

$$(4) \qquad G(s) = \frac{I_{BIAS} K_{ICO}}{s \cdot M} = \frac{K_{ICO}}{M \cdot s}\left[\frac{\int I_1 \cdot dt}{RC_1} \cdot \frac{g_m + 2s \cdot C_2}{g_m + s \cdot C_2} + I_{PROP} \cdot \frac{g_m}{g_m + s \cdot C_2}\right]$$

In Equation 4, K_{ICO} represents gain of CCO 18 in Hz/A, s represents a frequency of operation, M represents a PLL multiplier setting, and g_m represents transconductance of Mg_m. Clock dithering may be desirable in certain applications and undesirable in other applications, according to particular needs. In particular embodiments, to provide clock dithering, a suitable current addition and subtraction circuit may be added to current summer 16. The current addition and subtraction circuit may add or subtract current from the input to CCO 18 at a periodic rate to reduce power output of PLL 10. In particular embodiments, to provide clock dithering, a high-resistance transistor may be added to each CCO element 44. FIGURE 3 illustrates an example CCO element 44. In particular embodiments, to provide clock dithering, a high-resistance transistor may be added to CCO element 44, with the gate and the drain of

the transistor coupled to OUT– and the source of the transistor coupled to V_{DD}. The source current of the transistor may be approximately equal to I_{INT} divided by one hundred.

FIGURE 4 illustrates an example method for frequency correction in PLL 10. The method begins at step 100, where a frequency difference arises between comparison signal 28 and clock signal 24. At step 102, phase frequency detector 12 communicates the frequency difference to PI controller 14. At step 104, PI controller 14 adjusts current 32a to current summer 16 according to the frequency difference. At step 106, in response to the change in current 32a, current summer 16 adjusts control current 34 to CCO 18 to correct the frequency difference, at which point the method ends.

FIGURE 5 illustrates an example method for phase correction in PLL 10. The method begins at step 200, where a phase difference arises between comparison signal 28 and clock signal 24. At step 202, phase frequency detector 12 communicates a frequency difference to a loop filter cap. At step 204, the loop filter cap generates a voltage that is proportional to an integral of the frequency difference. The integral of the frequency difference corresponds to the phase difference. At step 206, V2I converter 42 generates a current that is proportional to the phase difference. At step 208, PI controller 14 adjusts current 32b to current summer 16 according to the phase difference. At step 210, in response to the change in current 32b, current summer 16 adjusts control current 34 to CCO 18 to correct the phase difference, at which point the method ends.

Although the methods illustrated in FIGURES 4 and 5 have been illustrated and described separately, these methods may be executed more or less simultaneously in PLL 10, using one or more of the same components, according to particular needs. Although the present invention has been described with several embodiments, myriad changes, variations, alterations, transformations, and modifications may be suggested to one skilled in the art, and it is intended that the present invention encompass such changes, variations, alterations, transformations, and modifications as fall within the

scope of the appended claims. The present invention is not intended to be limited, in any way, by any statement in the specification that is not reflected in the claims.